1. A method for etching a substrate, comprising:

placing a substrate into a reactive chamber;

introducing into said chamber an etching gas;

generating a plasma of said etching gas at a first power level and contacting said substrate with said first power level plasma for a first predetermined time; and,

generating a plasma of said etching gas at a second power level in said chamber and contacting said substrate with said second power level plasma for a second predetermined time, wherein said second power level plasma is a high power plasma and is greater than said first power level plasma, which is a low power plasma.

2. The method according to claim 1, wherein said low power plasma is from about 100 Watts to about 250 Watts.

3. The method according to claim 1, wherein said low power plasma is about 150 Watts.

4. The method according to claim 1, wherein said first predetermined time is from about 3 seconds to about 10 seconds.

5. The method according to claim 1, wherein said first predetermined time is about 5 seconds.

6. The method according to claim 1, wherein said high power plasma is from about 800 Watts to about 1100 Watts.

7. The method according to claim 1, wherein said high power plasma is about 950 Watts.

8. The method according to claim 1, wherein said second predetermined time is from about 30 seconds to about 260 seconds.

9. The method according to claim 1, wherein said second predetermined time is about 60 seconds.

10. The method according to claim 1, wherein said low power and said high power plasmas of said etching gas are selected from the group consisting of Cl_2, HBr, CF_4, CHF_3, CH_2F_2 and inert gases.

11. The method according to claim 10, wherein said low power plasma is CF_4, CHF_3 and an inert gas.

12. The method according to claim 10, wherein said high power plasma is CF_4, CHF_3 and an inert gas.

13. The method according to claim 10, wherein said low power and said high power plasmas are CF_4, CHF_3 and Ar.

14. The method according to claim 10, wherein said low power and said high power plasmas are CF_4, CHF_3 and He.

15. The method according to claim 1, wherein said substrate is a silicon-based substrate.

16. The method according to claim 15, wherein said substrate has an oxide layer formed over said substrate.

17. The method according to claim 1, wherein said substrate is a germanium substrate.

18. The method according to claim 17, wherein said substrate has an oxide layer formed over said substrate.

19. The method according to claim 1, wherein said substrate is a gallium arsenide substrate.

20. The method according to claim 19, wherein said substrate has an oxide layer formed over said substrate.

21. A method for reducing striations formed by the plasma etching of a substrate, comprising:

placing a substrate into a reactive chamber;

introducing into said chamber an etching gas;

generating a plasma of said etching gas at a first power level and contacting said substrate with said first power level plasma for a first predetermined time; and,

generating a plasma of said etching gas at a second power level in said chamber and contacting said substrate with said second power level plasma for a second predetermined time, wherein said second power level plasma is a high power plasma and is greater than said first power level plasma, which is a low power plasma.

22. The method according to claim 21, wherein said low power plasma is from about 100 Watts to about 250 Watts.

23. The method according to claim 21, wherein said low power plasma is about 150 Watts.

24. The method according to claim 21, wherein said first predetermined time is from about 3 seconds to about 10 seconds.

25. The method according to claim 21, wherein said first predetermined time is about 5 seconds.

26. The method according to claim 21, wherein said high power plasma is from about 800 Watts to about 1100 Watts.

27. The method according to claim 21, wherein said high power plasma is about 950 Watts.

28. The method according to claim 21, wherein said second predetermined time is from about 30 seconds to about 260 seconds.

29. The method according to claim 21, wherein said second predetermined time is about 60 seconds.

30. The method according to claim 21, wherein said low power and said high power plasmas of said etching gas are selected from the group consisting of Cl_2, HBr, CF_4, CHF_3, CH_2F_2 and inert gases.

31. The method according to claim 30, wherein said low power plasma is CF_4, CHF_3 and an inert gas.

32. The method according to claim 30, wherein said high power plasma is CF_4, CHF_3 and an inert gas.

33. The method according to claim 30, wherein said low power and said high power plasmas are CF_4, CHF_3 and Ar.

34. The method according to claim 30, wherein said low power and said high power plasmas are CF_4, CHF_3 and He.

35. The method according to claim 21, wherein said substrate is a silicon-based substrate.

36. The method according to claim 35, wherein said substrate has an oxide layer formed over said substrate.

37. The method according to claim 21, wherein said substrate is a germanium substrate.

38. The method according to claim 37, wherein said substrate has an oxide layer formed over said substrate.

39. The method according to claim 21, wherein said substrate is a gallium arsenide substrate.

40. The method according to claim 39, wherein said substrate has an oxide layer formed over said substrate.

41. A method for reducing CD loss in an etched semiconductor substrate, comprising:

placing a substrate into a reactive chamber;

introducing into said chamber an etching gas;

generating a plasma of said etching gas at a first power level and contacting said substrate with said first power level plasma for a time of from about 3 to about 10 seconds; and,

generating a plasma of said etching gas at a second power level in said chamber and contacting said substrate with said second power level plasma for a time of from about 20 to about 260 seconds, wherein said second power level plasma is a high power plasma and is greater than said first power level plasma, which is a low power plasma.

42. The method according to claim 41, wherein said low power plasma is from about 100 Watts to about 250 Watts.

43. The method according to claim 41, wherein said low power plasma is about 150 Watts.

44. The method according to claim 41, wherein said substrate is contacted with said low power plasma for about 5 seconds.

45. The method according to claim 41, wherein said high power plasma is from about 800 Watts to about 1100 Watts.

46. The method according to claim 41, wherein said high power plasma is about 950 Watts.

47. The method according to claim 41, wherein said substrate is contacted with said high power plasma for about 60 seconds.

48. The method according to claim 41, wherein said low power and said high power plasmas of said etching gas are selected from the group consisting of Cl_2, HBr, CF_4, CHF_3, CH_2F_2 and inert gases.

49. The method according to claim 48, wherein said low power plasma is CF_4, CHF_3 and an inert gas.

50. The method according to claim 48, wherein said high power plasma is CF_4, CHF_3 and an inert gas.

51. The method according to claim 48, wherein said low power and said high power plasmas are CF_4, CHF_3 and Ar.

52. The method according to claim 48, wherein said low power and said high power plasmas are CF_4, CHF_3 and He.

53. The method according to claim 41, wherein said substrate is a silicon-based substrate.

54. The method according to claim 53, wherein said substrate has an oxide layer formed over said substrate.

55. The method according to claim 41, wherein said substrate is a germanium substrate.

56. The method according to claim 55, wherein said substrate has an oxide layer formed over said substrate.

57. The method according to claim 41, wherein said substrate is a gallium arsenide substrate.

58. The method according to claim 57, wherein said substrate has an oxide layer formed over said substrate.

59. An integrated circuit substrate having improved CD loss and reduced striations formed by a method, comprising:

placing said integrated circuit substrate into a reactive chamber;

introducing into said chamber an etching gas;

generating a plasma of said etching gas at a first power level and contacting said substrate with said first power level plasma for a first predetermined time; and,

generating a plasma of said etching gas at a second power level in said chamber and contacting said integrated circuit substrate with said high power plasma for a second predetermined time, wherein said second power level plasma is a high power plasma and is greater than said first power level plasma, which is a low power plasma.

60. The integrated circuit substrate according to claim 59, wherein said substrate is a silicon-based substrate.

61. The integrated circuit substrate according to claim 60, wherein said substrate has an oxide layer formed over said substrate.

62. The integrated circuit substrate according to claim 59, wherein said substrate is a germanium substrate.

63. The integrated circuit substrate according to claim 62, wherein said substrate has an oxide layer formed over said substrate.

64. The integrated circuit substrate according to claim 59, wherein said substrate is a gallium arsenide substrate.

65. The integrated circuit substrate according to claim 64, wherein said substrate has an oxide layer formed over said substrate.

66. The integrated circuit substrate according to claim 65, wherein said substrate further has an antireflective coating thereon.

67. The integrated circuit substrate according to claim 59, wherein said substrate is a DRAM substrate.

68. The integrated circuit substrate according to claim 59, wherein said low power plasma is from about 100 Watts to about 250 Watts.

69. The integrated circuit substrate according to claim 59, wherein said low power plasma is about 150 Watts.

70. The integrated circuit substrate according to claim 59, wherein said first predetermined time is from about 3 seconds to about 10 seconds.

71. The integrated circuit substrate according to claim 59, wherein said first predetermined time is about 5 seconds.

72. The integrated circuit substrate according to claim 59, wherein said high power plasma is from about 800 Watts to about 1100 Watts.

73. The integrated circuit substrate according to claim 59, wherein said high power plasma is about 950 Watts.

74. The integrated circuit substrate according to claim 59, wherein said second predetermined time is from about 40 seconds to about 90 seconds.

75. The integrated circuit substrate according to claim 59, wherein said second predetermined time is about 60 seconds.

76. The integrated circuit substrate according to claim 59, wherein said low power and said high power plasmas of said etching gas are selected from the group consisting of Cl_2, HBr, CF_4, CHF_3, CH_2F_2, and inert gases.

77. The integrated circuit substrate according to claim 76, wherein said low power plasma is CH_4, CHF_3 and an inert gas.

78. The integrated circuit substrate according to claim 76, wherein said high power plasma is CF_4, CHF_3 and an inert gas.

79. The integrated circuit substrate according to claim 76, wherein said low power plasma includes HBr.

80. The integrated circuit substrate according to claim 76, wherein said high power plasma includes HBr.

81. The integrated circuit substrate according to claim 76, wherein said low power plasma includes Cl_2.

82. The integrated circuit substrate according to claim 76, wherein said high power plasma includes Cl_2.

83. The integrated circuit substrate according to claim 76, wherein said low power and said high power plasmas are CF_4, CHF_3 and Ar.

84. The integrated circuit substrate according to claim 76, wherein said low power and said high power plasmas are CF_4, CHF_3 and He.

85. A method for plasma etching a silicon substrate, comprising:

providing a silicon substrate having an oxide layer, a patterned photoresist layer, and an antireflective layer;

placing said substrate into a reactive chamber;

generating a first low power plasma of said etching gas in said chamber at about 100-200 Watts;

contacting said substrate with said low power plasma for a time of from about 3 to about 10 seconds to stabilize said patterned photoresist layer on said substrate;

generating a second high power plasma of said etching gas in said chamber at about 800-1100 Watts; and,

contacting said substrate with said high power plasma for a time of from about 30 to about 500 seconds to etch said substrate.

86. The method according to claim 85, wherein said low power plasma is about 150 Watts.

87. The method according to claim 85, wherein said substrate is contacted with said low power plasma for about 5 seconds.

88. The method according to claim 85, wherein said high power plasma is about 950 Watts.

89. The method according to claim 85, wherein said substrate is contacted with said high power plasma for about 60 seconds.

90. The method according to claim 85, wherein said low power plasma of said etching gas includes CF_4, CHF_3 and Ar.

91. The method according to claim 85, wherein high power plasma of said etching gas includes CF_4, CHF_3 and Ar.